CLAIMS

1. A vertical junction field effect transistor comprising:

a drain semiconductor portion;

a drift semiconductor portion placed on a principal surface of the drain semiconductor portion and having first, second, third, and fourth regions extending in a predetermined axial direction intersecting with the principal surface;

a buried semiconductor portion having a conductivity type opposite to a conductivity type of the drift semiconductor portion and placed on the first, second, and third regions of the drift semiconductor portion;

a channel semiconductor portion placed along the buried semiconductor portion, having the conductivity type opposite to the conductivity type of the buried semiconductor portion, and electrically connected to the fourth region of the drift semiconductor portion;

a source semiconductor portion placed on the channel semiconductor portion and the first region of the drift semiconductor portion; and

a gate semiconductor portion having a conductivity type opposite to a conductivity type of the drain semiconductor portion and placed on the channel semiconductor portion and the third and fourth

regions;

wherein the gate semiconductor portion has a plurality of projections extending in a direction from the third region toward the fourth region, the channel semiconductor portion is placed between the projections, and the projections are connected to the buried semiconductor portion.

2. A vertical junction field effect transistor comprising:

a drain semiconductor portion;

a drift semiconductor portion placed on a principal surface of the drain semiconductor portion and having first, second, third, and fourth regions extending in a predetermined axial direction intersecting with the principal surface;

a buried semiconductor portion having a conductivity type opposite to a conductivity type of the drift semiconductor portion and placed on the first, second, and third regions of the drift semiconductor portion;

a channel semiconductor portion placed along the buried semiconductor portion, having the conductivity type opposite to the conductivity type of the buried semiconductor portion, and electrically connected to the fourth region of the drift semiconductor portion;

a source semiconductor portion placed on the

channel semiconductor portion and the first region of the drift semiconductor portion; and

a plurality of gate semiconductor portions having a conductivity type opposite to a conductivity type of the drain semiconductor portion and placed on the channel semiconductor portion and the third and fourth regions;

wherein each of the gate semiconductor portions extends in a direction from the third region toward the fourth region, the channel semiconductor portion is placed between the gate semiconductor portions, and each gate semiconductor portion is connected to the buried semiconductor portion.

3. A vertical junction field effect transistor comprising:

a drain semiconductor portion;

a drift semiconductor portion placed on a principal surface of the drain semiconductor portion and having first, second, third, and fourth regions extending in a predetermined axial direction intersecting with the principal surface;

a buried semiconductor portion placed on a principal surface of the drift semiconductor portion and placed on the first, second, and third regions extending in the predetermined axial direction intersecting with the principal surface;

a channel semiconductor portion placed along the buried semiconductor portion, having a conductivity type opposite to a conductivity type of the buried semiconductor portion, and electrically connected to the fourth region of the drift semiconductor portion; and

a gate semiconductor portion having a conductivity type opposite to a conductivity type of the drift semiconductor portion and placed on the channel semiconductor portion and the third and fourth regions;

wherein the gate semiconductor portion has a plurality of projections extending in a direction from the third region toward the fourth region, the channel semiconductor portion is placed between the projections, and the drift semiconductor portion is connected to the buried semiconductor portion,

wherein the drift semiconductor portion has a fifth region extending in the axial direction intersecting with the principal surface of the drain semiconductor portion,

the transistor further comprising a second semiconductor portion having a conductivity type opposite to a conductivity type of the drain semiconductor portion and placed above the fifth region,

wherein the second semiconductor portion extends from the buried semiconductor portion in the predetermined axial direction along a source semiconductor portion.

4. The vertical junction field effect transistor according to any one of Claims 1 to 3, further comprising a first semiconductor portion placed on the channel semiconductor portion and the first and second regions of the drift semiconductor portion and having the same conductivity type as the source semiconductor portion,

wherein a dopant concentration of the first semiconductor portion is lower than a dopant concentration of the channel semiconductor portion.

5. A vertical junction field effect transistor comprising:

a drain semiconductor portion;

a drift semiconductor portion placed on a principal surface of the drain semiconductor portion and having first to fifth regions extending in a predetermined axial direction intersecting with a reference plane extending along the principal surface;

a buried semiconductor portion having a conductivity type opposite to a conductivity type of the drift semiconductor portion and placed along the reference plane on the first to fourth regions of the

drift semiconductor portion;

a plurality of gate semiconductor portions placed along the reference plane on the second to fourth regions of the drift semiconductor portion and having the same conductivity type as the conductivity type of the buried semiconductor portion;

a channel semiconductor portion placed between the buried semiconductor portion and the plurality of gate semiconductor portions, and between the plurality of gate semiconductor portions, and having the conductivity type opposite to the conductivity type of the buried semiconductor portion;

a connection semiconductor portion having the same conductivity type as the conductivity type of the buried semiconductor portion and the channel semiconductor portion, extending in the predetermined axial direction, and connecting the buried semiconductor portion and the plurality of gate semiconductor portions;

a first aggregate semiconductor portion connecting the channel semiconductor portion on the first region of the drift semiconductor portion;

a second aggregate semiconductor portion connecting the channel semiconductor portion on the fifth region of the drift semiconductor portion; and

a source semiconductor portion placed above the

first region of the drift semiconductor portion and connected to the first aggregate semiconductor portion.

6. A vertical junction field effect transistor comprising:

a drain semiconductor portion;

a drift semiconductor portion placed on a principal surface of the drain semiconductor portion and having first to fifth regions extending in a predetermined axial direction intersecting with a reference plane extending along the principal surface;

a buried semiconductor portion having a conductivity type opposite to a conductivity type of the drift semiconductor portion and placed along the reference plane on the first to fourth regions of the drift semiconductor portion;

a plurality of gate semiconductor portions placed along the reference plane on the second to fourth regions of the drift semiconductor portion and having the same conductivity type as the conductivity type of the buried semiconductor portion;

a channel semiconductor portion placed between the buried semiconductor portion and the plurality of gate semiconductor portions, and between the plurality of gate semiconductor portions, and having the conductivity type opposite to the conductivity type of the buried semiconductor portion;

a connection semiconductor portion having the same conductivity type as the conductivity type of the channel semiconductor portion and connecting the plurality of gate semiconductor portions;

a first aggregate semiconductor portion connecting the channel semiconductor portion on the first region of the drift semiconductor portion;

a second aggregate semiconductor portion connecting the channel semiconductor portion on the fifth region of the drift semiconductor portion; and

a source semiconductor portion placed above the first region of the drift semiconductor portion and connected to the first aggregate semiconductor portion;

wherein the drift semiconductor portion has a sixth region provided on a principal surface thereof and extending in the direction intersecting with the principal surface,

the transistor further comprising a third connection semiconductor portion having a conductivity type opposite to a conductivity type of the drain semiconductor portion and placed above the sixth region,

wherein the third connection semiconductor portion is placed along the first aggregate semiconductor portion.

7. The vertical junction field effect transistor

according to any one of Claims 1 to 4, wherein a thickness of the gate semiconductor portion and the channel semiconductor portion is smaller than a space between the source semiconductor portion and the buried semiconductor portion on the first region of the drift semiconductor portion.

8. The vertical junction field effect transistor according to Claim 5 or 6, wherein a thickness of the gate semiconductor portions and the channel semiconductor portion on the second to fourth regions of the drift semiconductor portion is smaller than a space between the source semiconductor portion and the buried semiconductor portion on the first region of the drift semiconductor portion.

9. The vertical junction field effect transistor according to any one of Claims 1, 2, and 4, wherein a space between the projections of the gate semiconductor portion is determined so that the vertical junction field effect transistor can exhibit the normally-off characteristic.

10. The vertical junction field effect transistor according to Claim 3, wherein a space between the projections of the gate semiconductor portion and a space between the projections of the gate semiconductor portion and the buried semiconductor portion are determined so that the vertical junction

field effect transistor can exhibit the normally-off characteristic.

11. The vertical junction field effect transistor according to any one of Claims 5 to 7, wherein a space between the gate semiconductor portions, and a space between the gate semiconductor portions and the buried semiconductor portion are determined so that the vertical junction field effect transistor can exhibit the normally-off characteristic.

12. The vertical junction field effect transistor according to any one of Claims 1 to 11, wherein the channel semiconductor portion has a structure in which low-concentration layers and high-concentration layers are alternately stacked.

13. The vertical junction field effect transistor according to any one of Claims 1 to 11, wherein the drift semiconductor portion has:

an electroconductive semiconductor region extending along a reference plane intersecting with the principal surface of the drain semiconductor portion, having the same conductivity type as the conductivity type of the drain semiconductor portion, and electrically connected to the channel semiconductor portion; and

a non-electroconductive semiconductor region placed next to the electroconductive semiconductor

region, having the conductivity type opposite to the conductivity type of the drain semiconductor portion, and electrically connected to the buried semiconductor portion; and

wherein the electroconductive semiconductor region and the non-electroconductive semiconductor region are formed in the same direction as a direction in which the first to fourth regions of the drift semiconductor portion are arranged.

14. The vertical junction field effect transistor according to any one of Claims 1 to 11, wherein the drift semiconductor portion has:

an electroconductive semiconductor region extending along a reference plane intersecting with the principal surface of the drain semiconductor portion, having the same conductivity type as the conductivity type of the drain semiconductor portion, and electrically connected to the channel semiconductor portion; and

a non-electroconductive semiconductor region placed next to the electroconductive semiconductor region, having the conductivity type opposite to the conductivity type of the drain semiconductor portion, and electrically connected to the buried semiconductor portion; and

wherein the electroconductive semiconductor

region and the non-electroconductive semiconductor region are formed in a direction intersecting with a direction in which the first to fourth regions of the drift semiconductor portion are arranged.

15. The vertical junction field effect transistor according to any one of Claims 1 to 14, wherein the drain semiconductor portion, the drift semiconductor portion, the buried semiconductor portion, the gate semiconductor portion, the channel semiconductor portion, the connection semiconductor portion, and the source semiconductor portion are made of SiC or GaN which is a wide-gap semiconductor material.

16. A method of producing a vertical junction field effect transistor, comprising:

a step of forming a first semiconductor layer of a first conductivity type on a substrate of the first conductivity type, wherein a principal surface of the first semiconductor layer has first to fourth regions arranged in order in a predetermined axial direction;

a step of introducing a dopant of a second conductivity type into the first to third regions of the principal surface of the first semiconductor layer to form a buried semiconductor portion;

a step of forming a second semiconductor layer of the first conductivity type on the first semiconductor

layer;

a step of forming a source semiconductor layer of the first conductivity type on the second semiconductor layer;

a step of etching the source semiconductor layer above at least one of the second, third, and fourth regions of the principal surface of the first semiconductor layer, up to the first semiconductor layer to expose a predetermined region of the second semiconductor layer,

wherein the predetermined region has a plurality of first portions extending in the predetermined axial direction, and a second portion defined so as to embrace the plurality of portions; and

a step of introducing a dopant of the second conductivity type for a gate semiconductor portion into the plurality of first portions to form a first semiconductor portion of the second conductivity type.

17. The method according to Claim 16, further comprising a step of introducing a dopant of the second conductivity type for the gate semiconductor portion into the second portion to form a second semiconductor portion of the second conductivity type,

wherein a depth of the second semiconductor portion is smaller than a depth of the first semiconductor portion.

18. The method according to Claim 16 or 17, wherein the first semiconductor portion is formed so as to be connected to the buried semiconductor portion.

19. A method of producing a vertical junction field effect transistor, comprising:

a first semiconductor layer forming step of forming a first semiconductor layer of a first conductivity type on a substrate of the first conductivity type,

wherein a principal surface of the first semiconductor layer has first to fourth regions arranged in order in a predetermined axial direction;

a buried semiconductor portion forming step of introducing a dopant of a second conductivity type into the first to third regions of the principal surface of the first semiconductor layer to form a buried semiconductor portion;

a second semiconductor layer forming step of forming a second semiconductor layer of the first conductivity type on the first semiconductor layer;

a second semiconductor region step of introducing a dopant of the second conductivity type for a gate semiconductor portion into the second semiconductor layer on the second and third regions of the principal surface of the first semiconductor layer up to a predetermined depth to form a second semiconductor

region of the second conductivity type;

a channel semiconductor portion forming step of repeating the second semiconductor layer forming step and the second semiconductor region step before obtaining a desired number of said second semiconductor layers, to form a stack of gate semiconductor portions and channel semiconductor portions; and

a source semiconductor portion forming step of forming a source semiconductor portion on the channel semiconductor portion.

20. The method according to Claim 19, wherein the second semiconductor layer forming step comprises forming the second semiconductor layer of the first conductivity type in a predetermined thickness on the first semiconductor layer, and

wherein the channel semiconductor portion forming step comprises introducing the dopant of the second conductivity type so as to achieve a maximum concentration in a predetermined depth in the second semiconductor layer, thereby forming the stack of gate semiconductor portions and channel semiconductor portions.

21. The method according to Claim 20, wherein the channel semiconductor portion forming step comprises alternately introducing a first dopant and a second dopant so as to achieve a maximum concentration

in a predetermined depth in the second semiconductor layer, thereby forming the stack of gate semiconductor portions and channel semiconductor portions.

22. The method according to any one of Claims 19 to 21, wherein the channel semiconductor portion forming step comprises a connection region forming step of forming a second semiconductor connection region of the second conductivity type so as to connect interiors of the second semiconductor layers to each other.

23. The method according to any one of Claims 16 to 22, wherein the step of forming the first semiconductor layer comprises forming the first semiconductor layer so as to form an electroconductive semiconductor layer of the same conductivity type as the substrate of the first conductivity type, form a non-electroconductive semiconductor layer of the conductivity type opposite to that of the electroconductive semiconductor layer, on the electroconductive semiconductor layer, and electrically connect the electroconductive semiconductor layer to the channel semiconductor portion.

24. The method according to any one of Claims 16 to 22, wherein the step of forming the first semiconductor layer comprises forming the first semiconductor layer so as to form a non-electroconductive semiconductor layer of the

conductivity type opposite to the substrate of the first conductivity type, form an electroconductive semiconductor layer of the conductivity type opposite to that of the non-electroconductive semiconductor layer, on the non-electroconductive semiconductor layer, and electrically connect the electroconductive semiconductor layer to the channel semiconductor portion.

25. The method according to any one of Claims 16 to 22, wherein the step of forming the first semiconductor layer comprises forming the electroconductive semiconductor layer and the non-electroconductive semiconductor layer in a direction intersecting with the principal surface of the substrate, thereby forming the first semiconductor layer.

26. The vertical junction field effect transistor according to Claim 3, further comprising a source electrode electrically connected to the source semiconductor portion and the second semiconductor portion, wherein the buried semiconductor portion is electrically connected through the second semiconductor portion to the source electrode.

27. A vertical junction field effect transistor comprising:

a drain semiconductor portion;

a drift semiconductor portion placed on a principal surface of the drain semiconductor portion and having first, second, third, and fourth regions extending in a direction intersecting with the principal surface;

a buried semiconductor portion having a conductivity type opposite to a conductivity type of the drift semiconductor portion and placed on the first, second, and fourth regions of the drift semiconductor portion;

a channel semiconductor portion placed along the buried semiconductor portion on the first and second regions, having a conductivity type different from the conductivity type of the buried semiconductor portion, and electrically connected to the third region of the drift semiconductor portion;

a source semiconductor portion placed on the channel semiconductor portion and the first region of the drift semiconductor portion;

a first gate semiconductor portion having the same conductivity type as the buried semiconductor portion, electrically connected to the buried semiconductor portion, and placed above the fourth region of the drift semiconductor portion;

a first gate electrode electrically connected to the first gate semiconductor portion above the fourth

region of the drift semiconductor portion; and

a source electrode electrically connected to the source semiconductor portion above the first region of the drift semiconductor portion, electrically isolated from the first gate electrode above the first gate electrode, and placed above the first, second, third, and fourth regions of the drift semiconductor portion.

28. The vertical junction field effect transistor according to Claim 27, further comprising a second gate semiconductor portion having a conductivity type opposite to a conductivity type of the drain semiconductor portion and placed above the second region or above the second and third regions of the drift semiconductor portion,

wherein the channel semiconductor portion is placed between the buried semiconductor portion and the second gate semiconductor portion, and

wherein a second gate electrode electrically connected to the second gate semiconductor portion and electrically isolated under the source electrode is placed above the second region or above the second and third regions of the drift semiconductor portion.

29. A vertical junction field effect transistor comprising:

a drain semiconductor portion;

a drift semiconductor portion placed on a

principal surface of the drain semiconductor portion and having first, second, third, and fourth regions extending in a direction intersecting with the principal surface;

a buried semiconductor portion having a conductivity type opposite to a conductivity type of the drift semiconductor portion and placed on the first, second, and fourth regions of the drift semiconductor portion;

a channel semiconductor portion placed along the buried semiconductor portion on the first and second regions, having a conductivity type different from the conductivity type of the buried semiconductor portion, and electrically connected to the third region of the drift semiconductor portion;

a source semiconductor portion placed on the channel semiconductor portion and the first region of the drift semiconductor portion;

a first gate semiconductor portion having the same conductivity type as the buried semiconductor portion, electrically connected to the buried semiconductor portion, and placed above the fourth region of the drift semiconductor portion;

a source electrode electrically connected to the source semiconductor portion above the first region of the drift semiconductor portion, electrically isolated

from the first gate electrode above the first gate electrode, and placed above the first, second, third, and fourth regions of the drift semiconductor portion; and

a second gate semiconductor portion having a conductivity type opposite to a conductivity type of the drain semiconductor portion and placed above the second region or above the second and third regions of the drift semiconductor portion;

wherein the channel semiconductor portion is placed between the buried semiconductor portion and the second gate semiconductor portion,

wherein a second gate electrode electrically connected to the second gate semiconductor portion and electrically isolated under the source electrode is placed above the second region or above the second and third regions of the drift semiconductor portion, and

wherein the first gate semiconductor portion and the source semiconductor portion are electrically connected by the source electrode.

30. A vertical junction field effect transistor comprising:

a drain semiconductor portion;

a drift semiconductor portion placed on a principal surface of the drain semiconductor portion and having first, second, and third regions extending

in a direction intersecting with the principal surface;

a buried semiconductor portion having a conductivity type opposite to a conductivity type of the drift semiconductor portion and placed on the first, second, and third regions of the drift semiconductor portion;

a channel semiconductor portion placed along the buried semiconductor portion on the first and second regions, having a conductivity type different from the conductivity type of the buried semiconductor portion, and electrically connected to the third region of the drift semiconductor portion;

a source semiconductor portion placed on the channel semiconductor portion and the first region of the drift semiconductor portion;

a second gate semiconductor portion having a conductivity type opposite to a conductivity type of the drain semiconductor portion and placed above the second region or above the second and third regions of the drift semiconductor portion;

a second gate electrode placed above the second region or above the second and third regions of the drift semiconductor portion, electrically connected to the second gate semiconductor portion, and electrically isolated under the source electrode;

a source electrode electrically connected to the

source semiconductor portion above the first region of the drift semiconductor portion, electrically isolated from the second gate electrode above the second gate electrode, and placed above the first, second, and third regions of the drift semiconductor portion; and

connection semiconductor portions having the same conductivity type as the buried semiconductor portion, penetrating the channel semiconductor portion so as to electrically connect the second gate semiconductor portion and the buried semiconductor portion, and scattered above the second region of the drift semiconductor portion.

31. The vertical junction field effect transistor according to any one of Claims 27 to 30, further comprising a first semiconductor portion placed on the channel semiconductor portion and the first region of the drift semiconductor portion and having the same conductivity type as a conductivity type of the source semiconductor portion,

wherein an impurity concentration of the first semiconductor portion is lower than an impurity concentration of the channel semiconductor portion.

32. The vertical junction field effect transistor according to any one of Claims 27 to 31, wherein at least one of the first and second gate electrodes is provided as a gate electrode in a

peripheral portion of a primitive cell or chip comprised of a plurality of transistors.

33. The vertical junction field effect transistor according to Claim 6, wherein the first gate semiconductor portion and the source semiconductor portion are electrically connected by the source electrode, to a peripheral portion of a primitive cell or chip comprised of a plurality of transistors.

34. The vertical junction field effect transistor according to any one of Claims 28 to 33, wherein the second gate semiconductor portion and the channel semiconductor portion are provided so as to constitute a heterojunction.

35. The vertical junction field effect transistor according to any one of Claims 27 to 34, wherein a thickness of the channel semiconductor portion placed above the second region of the drift semiconductor portion is smaller than a space between the source semiconductor portion and the buried semiconductor portion placed on the first region of the drift semiconductor portion.

36. The vertical junction field effect transistor according to any one of Claims 27 to 35, wherein a thickness of the channel semiconductor portion placed above the second region of the drift semiconductor portion is determined so that the

vertical junction field effect transistor can exhibit the normally-off characteristic.

37. The vertical junction field effect transistor according to any one of Claims 27 to 36, wherein the channel semiconductor portion has a structure in which low-concentration layers and high-concentration layers are alternately stacked.

38. The vertical junction field effect transistor according to any one of Claims 27 to 37, wherein the drift semiconductor portion has an electroconductive semiconductor region extending along a reference plane intersecting with the principal surface of the drain semiconductor portion, having the same conductivity type as the drain semiconductor portion, and electrically connected from the third region of the drift semiconductor portion to the channel semiconductor portion; and

a non-electroconductive semiconductor region placed next to the electroconductive semiconductor region, having the conductivity type opposite to the conductivity type of the drain semiconductor portion, and electrically connected to the buried semiconductor portion; and

wherein the electroconductive semiconductor region and the non-electroconductive semiconductor region are formed in the same direction as a direction

in which the first to fourth regions of the drift semiconductor portion are arranged.

39. The vertical junction field effect transistor according to any one of Claims 27 to 37, wherein the drift semiconductor portion has an electroconductive semiconductor region extending along a reference plane intersecting with the principal surface of the drain semiconductor portion, having the same conductivity type as the drain semiconductor portion, and electrically connected from the third region of the drift semiconductor portion to the channel semiconductor portion; and

a non-electroconductive semiconductor region placed next to the electroconductive semiconductor region, having the conductivity type opposite to the conductivity type of the drain semiconductor portion, and electrically connected to the buried semiconductor portion; and

wherein the electroconductive semiconductor region and the non-electroconductive semiconductor region are formed in a direction intersecting with a direction in which the first to fourth regions of the drift semiconductor portion are arranged.

40. The vertical junction field effect transistor according to any one of Claims 27 to 39, wherein the drain semiconductor portion, the drift

semiconductor portion, the first gate semiconductor portion, and the channel semiconductor portion are made of SiC or GaN which is a wide-gap semiconductor material.

41. A method of producing a vertical junction field effect transistor, comprising:

a step of forming a drift semiconductor layer having first, second, third, and fourth regions, on a substrate of a first conductivity type;

a step of introducing an impurity of a conductivity type opposite to a conductivity type of the drift semiconductor layer, into the first, second, and fourth regions of the drift semiconductor layer to form a buried semiconductor portion;

a step of forming a channel semiconductor portion having a conductivity type different from the conductivity type of the buried semiconductor portion, on the buried semiconductor portion and the drift semiconductor layer;

a step of forming a source semiconductor portion above the first region of the drift semiconductor layer;

a step of introducing an impurity of the same conductivity type as the conductivity type of the buried semiconductor portion, into a portion above the fourth region of the drift semiconductor layer to form

a first gate semiconductor portion;

a step of forming a first gate electrode electrically connected to the first gate semiconductor portion;

a step of forming an interlayer film electrically isolated from the first gate electrode; and

a step of forming a source electrode electrically connected to the source semiconductor portion, on the interlayer film.

42. The method according to Claim 41, further comprising:

a step of introducing an impurity of the same conductivity type as the conductivity type of the first gate semiconductor portion, into the second region or into the second and third regions of the drift semiconductor layer, prior to the step of forming the first gate semiconductor portion, to form a second gate semiconductor portion,

wherein a second gate electrode electrically connected to the second gate semiconductor portion is formed in the step of forming the first gate electrode.

43. A method of producing a vertical junction field effect transistor, comprising:

a step of forming a drift semiconductor layer having first, second, third, and fourth regions, on a substrate of a first conductivity type;

a step of introducing an impurity of a conductivity type opposite to a conductivity type of the drift semiconductor layer, into the first, second, and fourth regions of the drift semiconductor layer to form a buried semiconductor portion;

a step of forming a channel semiconductor portion having a conductivity type different from the conductivity type of the buried semiconductor portion, on the buried semiconductor portion and the drift semiconductor layer;

a step of forming a source semiconductor portion above the first region of the drift semiconductor layer;

a step of introducing an impurity of the same conductivity type as the conductivity type of the buried semiconductor portion, into the second region or into the second and third regions of the drift semiconductor layer to form a second gate semiconductor portion;

a step of introducing an impurity of the same conductivity type as the conductivity type of the buried semiconductor portion, into a portion above the fourth region of the drift semiconductor layer to form a first gate semiconductor portion;

a step of forming a second gate electrode electrically connected to the second gate semiconductor

portion; and

a step of forming a source electrode electrically connecting the source semiconductor portion and, a first semiconductor portion placed on the channel semiconductor portion and the first region of the drift semiconductor layer and having the same conductivity type as the source semiconductor portion.

44. A method of producing a vertical junction field effect transistor, comprising:

a step of forming a drift semiconductor layer having first, second, third, and fourth regions, on a substrate of a first conductivity type;

a step of introducing an impurity of a conductivity type opposite to a conductivity type of the drift semiconductor layer, into the first, second, and fourth regions of the drift semiconductor layer to form a buried semiconductor portion;

a step of forming a channel semiconductor portion having a conductivity type different from the conductivity type of the buried semiconductor portion, on the buried semiconductor portion and the drift semiconductor layer;

a step of forming a source semiconductor portion above the first region of the drift semiconductor layer;

a step of introducing an impurity having the same

conductivity type as the conductivity type of the buried semiconductor portion, into the second region or into the second and third regions of the drift semiconductor layer to form a second gate semiconductor portion;

a step of introducing an impurity of the same conductivity type as the conductivity type of the buried semiconductor portion, into portions above the second region of the drift semiconductor layer to form connection semiconductor portions connecting the second gate semiconductor portion and the buried semiconductor portion, in a scattered state; and

a step of forming a second gate electrode electrically connected to the second gate semiconductor portion.

45. The method according to any one of Claims 41 to 44, further comprising:

a step of forming a first semiconductor portion having the same conductivity type as the source semiconductor portion, on the channel semiconductor portion, prior to the step of forming the source semiconductor portion,

wherein an impurity concentration of the first semiconductor portion is lower than an impurity concentration of the channel semiconductor portion.

46. The method according to any one of Claims

41, 43, and 44, wherein the step of forming the drift semiconductor layer comprises forming the drift semiconductor layer so as to form an electroconductive semiconductor layer of the same conductivity type as the drain semiconductor portion, form a non-electroconductive semiconductor layer of the conductivity type opposite to that of the electroconductive semiconductor layer, in the electroconductive semiconductor layer, and electrically connect the electroconductive semiconductor layer to the channel semiconductor portion.

47. The method according to any one of Claims 41, 43, and 44, wherein the step of forming the drift semiconductor layer comprises forming the drift semiconductor layer so as to form a non-electroconductive semiconductor layer of the conductivity type opposite to that of the drift semiconductor portion, form an electroconductive semiconductor layer of the conductivity type opposite to that of the non-electroconductive semiconductor layer, in the non-electroconductive semiconductor layer, and electrically connect the electroconductive semiconductor layer to the channel semiconductor portion.